



Attorney Docket No.: PATENT
AHA-02101

2621
#61
BT
9-27-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:) Art Unit: 2621
Eric John Hewitt et al.) Examiner:
Serial No.: 09/808,884)
Filed: March 14, 2001) TRANSMITTAL LETTER
For: ENHANCED TURBO PRODUCT) 162 N. Wolfe Road
CODES) Sunnyvale, CA 90486
(408) 530-9700

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Technology Center 2800

Sir:

Enclosed please find a Supplemental Information Disclosure Statement, Form PTO-1449, copies of the references contained thereon, for filing in the U.S. Patent and Trademark Office.

The Commissioner is hereby authorized to charge any additional fee or credit overpayment to our Deposit Account No. 08-1275. An originally executed duplicate transmittal is enclosed for this purpose.

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Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: September 9, 2002

By: Jonathan O. Owens
Jonathan O. Owens
Reg. No.: 37,902

Attorneys for Applicants

CERTIFICATE OF MAILING (37 CFR § 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington D.C. 20231

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HAVERSTOCK & OWENS LLP

Date: 9/9/02 By: [Signature]



PATENT
Attorney Docket No.: AHA-02101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Eric John Hewitt et al.

Serial No.: 09/808,884

Filed: March 14, 2001

For: **ENHANCED TURBO PRODUCT
CODES**

) Group Art Unit: 2621

) Examiner:

) **SUPPLEMENTAL INFORMATION**
) **DISCLOSURE STATEMENT**

) 162 N. Wolfe Road
) Sunnyvale, CA 94086
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Washington, D.C. 20231

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The citations listed below, copies attached, may be material to the examination of the above-identified application, and are therefore submitted in compliance with the duty of disclosure defined in 37 C.F.R. §§ 1.56 and 1.97. The Examiner is requested to make these citations of official record in this application.

Applicant has become aware of the following printed publication which may be material to the examination of this application:

- U.S. Patent 5,541,955;
- U.S. Patent 6,104,758;
- "Diagnosing On-Card Error Checking and Correcting Operations Using Latched Syndrome Data, IBM Technical Disclosure Bulletin, October 1989, No. NA891026; and
- "Single-Bit Correct, Double-Bit Error Checking/Correction Scheme," IBM Technical Disclosure Bulletin, May 1994, No. NN9405101.

This Supplemental Information Disclosure Statement under 37 C.F.R. §§ 1.56 and 1.97 is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that anyone or more of these citations constitutes prior art.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: September 4, 2002

By: Jonathan O. Owens
Jonathan O. Owens
Reg. No.: 37, 902

Attorneys for Applicants

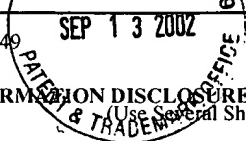
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HAVERSTOCK & OWENS LLP.

Date: 9/9/02 By: [Signature]

FORM PTO-1449 (Modified)				U.S. Department of Commerce Patent and Trademark Office		Attorney Docket No.: AHA-02101		Serial No.: 09/808,884	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use Several Sheets If Necessary)						Applicant: Eric Hewitt, <i>et al.</i>			
(37 CFR § 1.98(b))						Filing Date: March 14, 2001		Group Art Unit: 2621	
U.S. PATENT DOCUMENTS									
Examiner Initials		Serial / Patent Number	Issue Date	Applicant / Patentee	Class	Subclass	Filing Date		
	AA	5,541,955	07/30/96	Jacobsmeier	375	222	04/28/95		
	AB	6,104,758	08/15/00	Kaku et al.	375	265	09/09/97		
	AC								
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FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS									
		Document 628 Number	Publication Date	Country / Patent Office	Class	Subclass	Translation		
							Yes	No	
	AK								
	AL								
	AM								
	AN								
	AO								
OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication)									
	AP	"Diagnosing On-Card Error Checking and Correcting Operations Using Latched Syndrome Data, IBM Technical Disclosure Bulletin, October 1989, No. NA891026.							
	AQ	"Single-Bit Correct, Double-Bit Error Checking/Correction Scheme," IBM Technical Disclosure Bulletin, May 1994, No. NN9405101.							
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Examiner:					Date Considered:				
EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.									

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